5th Workshop on SoCs, Heterogeneous Architectures and Workloads
(SHAW- 5)

February 16th 2014, Florida, USA
Held in conjunction with HPCA-20

Organizing Chairs:

Ramesh Illikkal	Intel	ramesh.g.illikkal@intel.com
Ravi Iyer	Intel Labs	ravishankar.iyer@intel.com
Raj Yavatkar	Intel	raj.yavatkar@intel.com
Renato Figueiredo	University of Florida	renato@acis.ufl.edu

SHAW 2014 - Final Program

9:00 AM	9:05 AM	**Workshop Introduction & Opening remarks**		
9:05 AM	9:40 AM	**A Future Evolution in the Dimensionality of Systems Architecture (Invited talk)**	Dr. Phil Emma, Chief Scientist	IBM Research
9:40 AM	10:05 AM	Hardware Acceleration of Sparse Matrix-Vector Multiply	Bong Jin Ko†‡ Jin Min Kim‡ Kyungsang Cho†‡ Jae W. Lee‡	†Samsung Electronics ‡Sungkyunkwan University Yongin, Korea Suwon, Korea
10:05 AM	**10:35 AM**	**Break**		
10:35 AM	11:00 AM	A Low-power Neural Network using Approximate Computing	Somnath Paul, Julio C Zamora Esquivel , Caleb Lo, Charles Augustine, Li Zhao	Intel Corporation
11:00 AM	11:25 AM	A New Composite CPU/Memory Model for Predicting Efficiency of Multi-core Processing	Khondker S. Hasan, John K. Antonio, and Sridhar Radhakrishnan	School of Computer Science University of Oklahoma Norman, OK, USA
11:25 AM	11:50 AM	Performance Predication Model for Heterogeneous Multicore Architectures : A Machine Learning Approach	Bin Li*, Li Zhao*, Andrew Herdrich* and Sada Srinivasan §	*Intel Labs, Hillsboro, OR, U.S.A. §AMD, Austin, TX, U.S.A.
11:50 AM	**1:30 PM**	**Lunch break**		
1:30 PM	2:05 PM	**Synergistic Power-Management and QoS in Future Chip-Multiprocessors (Invited talk)**	Dr. Paul V. Gratz	Department of Electrical and Computer Engineering at Texas A&M University
2:05 PM	2:30 PM	A Transparent Multiple-ISA MPSoC Architecture	Anderson Sartor, Fernanda M. Capella, Marcelo Brandalero, Luigi Carro, Antonio C. S. Beck	Instituto de Informática - Universidade Federal do Rio Grande do Sul - Porto Alegre, Brazil
2:30 PM	2:55 PM	Trustworthy SoC Architecture with On-Demand Security Policies and HW-SW Cooperation	Yier Jin[1] and Daniela Oliveira[2]	[1]Department of Electrical Engineering and Computer Science, University of Central Florida [2]Department of Computer Science, Bowdoin College
2:55 PM	**3:30 PM**	**Break**		
3:30 PM	4:05 PM	**OpenCL High-Level Synthesis for Mainstream FPGA Acceleration**	Dr. Greg Stitt	University of Florida
4:05 PM	4:30 PM	Using monitors to predict co-running safety-critical hard real-time benchmark behavior	Jingyi Bin∗†, Sylvain Girbal†, Daniel Gracia P´erez† and Alain Merigot∗	∗Fundamental Electronic Institute, France †Thales Research & Technology, France
4:30 PM	4:55 PM	Profiling EEMBC MultiBench Programs using Full-system Simulations	Chao Chen[1], Ajay Joshi[1], and Erno Salminen[2]	[1]Electrical and Computer Engineering Department, Boston University, Boston, MA [2]Department of Pervasive Computing, Tampere University of Technology, Finland