5th Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW-5)

February 16th 2014, Orlando, Florida
Held in conjunction with HPCA-20
http://hpca20.ece.ufl.edu/shaw5.html

SHAW-5: CALL FOR PAPERS

Computing platforms are getting smaller (e.g. handheld devices, wearables), richer (e.g. image and language understanding) and broader (i.e. reaching the masses via Internet of Things). This trend is made possible by System-on-Chip (SoC) and Heterogeneous Architectures that combine wider power/performance scaling, combinations of high performance and ultra-low power general-purpose cores along with a wide spectrum of domain-specific accelerators or Intellectual Property (IP) blocks. With the recent introduction of general-purpose compute cores such as Intel® Core™ i7 and Atom™ processors and the recently announced Quark processor, these heterogeneous platforms have the potential to run a much broader range of applications than ever before. The goal of this workshop is to bring together academic researchers and industry practitioners to discuss future SoC and Heterogeneous architectures, Accelerators and Workloads. The research challenges in SoC/Heterogeneous platforms are multi-fold: (a) providing rich functionality and wider power/performance range (b) attempting to cover a broad range of applications that can be migrated from mainstream platforms to SoCs and Heterogeneous devices, (c) enabling a modular architecture and design environment that improves time-to-market and (d) providing a rich software programming environment that eases the challenge of developing applications on a heterogeneous architecture consisting of general-purpose cores as well as specialized accelerators.

Below is the proposed list of topics for the workshop. Topics include, but are not restricted to, the following:

- **Novel SoC/Hetero Architectures**
  - Architectures for wearable and IOT devices
  - Heterogeneity in Cores, Frequency, Cache, Memory
  - Different levels of Heterogeneity
  - Power, Performance, Energy optimizations
  - SoCs, CPU/GPU, CPU/GPGPU architectures
  - End-to-end heterogeneity (device-cloud offloads)
  - Ultra-Low Power Core Micro-architectures
  - Fabrics / Network-on-chip, Cache/Memory Hierarchies
  - HW Support for Heterogeneity, Programmability, Modularity
  - Simulation / Emulation Methodologies
- **Emerging Workloads and Embedded Devices**
  - New Workloads (Wearable/IOT usages)
  - Speech/Image recognition and understanding, Cognitive computing
  - Personal Assistants, Predictive/Prescriptive Analytics
  - Machine Learning Algorithms & Applications
  - Graph processing, Deep Neural Networks
  - Emerging embedded applications, devices and novel uses cases
  - Workload Analysis for power/performance/energy optimization and acceleration
  - Workload Partitioning between Heterogeneous Cores and Accelerators
  - Performance Monitoring and Simulation
  - Case Studies of SoC/Heterogeneous applications
- **Novel Accelerator Designs**
  - Specialized Accelerator Architectures and Designs
  - Machine Learning, Neural Network and Graph Processing accelerators
  - Domain-Specific Programmable/Configurable Accelerators
  - Accelerator Interfaces for Programmability
  - Development Environments for Accelerator Design

Submission Guidelines: Interested authors are encouraged to submit extended abstracts (1 - 2 pages) or short papers (6 pages) by email to the organizing chairs. The deadline for submission is December 23rd. Final (short) papers will be due on Jan 31st, 2014 and will be printed in a workshop proceedings made available to the workshop attendees.

Organizing Chairs

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Important dates

Abstract/Paper submission
~~December 16, 23:59 PST~~
December 23, 23:59 PST

Author Notification
January 10, 2014

Final Paper Submission
Jan 31, 2014

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Orlando, Florida
February 16, 2014